Static Magnetic Storage and Delay Line

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Static Magnetic Storage and Delay Line*,**

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Magnetic cores with a rectangular hysteresis loop are used in a storage system which requires no mechanical motion and is permanent. The binary digit "1" is stored as a positive residual flux, and the binary digit "0" as a residual flux in the opposite direction. When a negative probing field is applied to the core, a large voltage is induced in another winding if the digit stored has been a "1," and very small voltage if it has been a "0." The induced voltage in the former case is large enough to magnetize another core of identical construction. Binary digits can thus be transferred from one core into another. Many cores are arranged in tandem to form an information delay line. Binary digits can be advanced along the line step by step. The present upper limit of the speed of propagation is about 35,000 digits per second, and there is no lower limit.

I. INTRODUCTION

ONE of the most important research problems in the field of large-scale digital calculating machines is that of information storage. Electronic trigger pair tubes, cathode-ray tubes, acoustic delay lines, rotating drums, or tapes are used in present machines. Electronic trigger pair storage is, of course, the most versatile, but it is extremely expensive and its reliability poor. Cathode-ray tube and acoustic delay line storage systems need constant regeneration to preserve the information stored. All three systems lose the information if there is interruption of power. Magnetic drum or tape storage preserves information indefinitely, but it involves a mechanical system, and the operating speed is limited by mechanical considerations. Both in acoustic delay lines and rotating magnetic drums, the operation is necessarily synchronous. The speed depends upon the physical nature of the system and cannot be changed at will during operation.

This paper describes a storage system which operates like electronic trigger pairs but does not use vacuum tubes other than a relatively small number for control purposes.

A binary digit which takes the value of "0" or "1" is stored in a ferromagnetic core in the form of positive or negative residual magnetism, depending on the direction of the last magnetizing force. As shown in Fig. 1, a binary digit is represented by the point "0" or "1" on the hysteresis curve of the core. To store a binary digit, only the application of a magnetizing pulse of proper polarity is necessary.

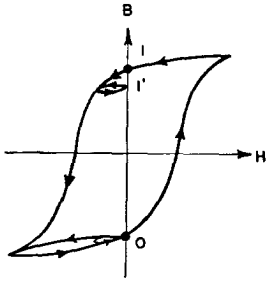

FIG. 1. Hysteresis loop.

The reading out of the stored information presents a more difficult problem. For a small negative pulse of magnetizing force H, applied at point "0," there results less change in the flux density B than for a similar negative pulse applied at point "1." Thus the relative amplitude of the induced voltage indicates what information has been stored in the material. However, this is true only for the first-read-out pulse, since after "0" information has been read out, the material returns to the point "0," whereas after "1" information has been read out, the material goes to a new point "1'" instead of returning to "1." Further negative pulses of H produce very nearly equal changes of B for starting positions "0" and "1'." Thus, whereas small read-out pulses do not actually destroy the positive or negative residual magnetism representing the stored information, they make reading out by like pulses impossible after the first.

When a large negative read-out pulse of H is impressed, the information is destroyed. The state of the material returns to position "0" in the B–H curve, no matter what information was previously stored. However, the secondary induced voltage is much larger when B changes from "1" to "0" than when B changes from "0" to "0." The ratio of these voltages was found to be as high as 30:1 for suitable magnetic materials. The large induced voltage can be made to drive another core from state "0" to "1." Thus one can construct (1) a storage unit in which digits can be stored and read-out continuously, and (2) an information delay line in which a series of binary digits can be propagated at

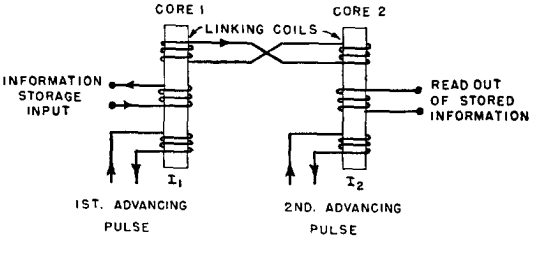

FIG. 2. Two-core storage unit.

* Work done under Contract W19-122-ac-24 between Harvard University and the United States Air Force.

** Presented at the Cambridge Meeting of the American Physical Society (June, 1949).

any desirable speed up to about thirty thousand information pulses per second.

II. A SINGLE-INFORMATION STORAGE UNIT

Since the large secondary induced voltage is sufficient to drive another core of similar size to its saturation, a means is available to transfer the information.[1] Such a storage unit is shown in Fig. 2. Core 1 and Core 2 are wound of strips of material with a nearly rectangular hysteresis loop to insure that the states of residual magnetism, 1 and 0, are well defined and stable. Assume

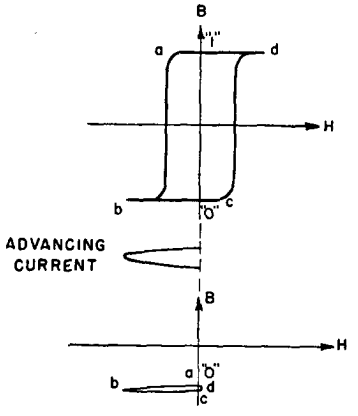

FIG. 3. Flux changing path.

that the 1 state of residual magnetism corresponds to flux in the cores in the upward direction, and the 0 state to flux in the downward direction. Then, whenever a 1 is stored in Core 1 through the information input coil, the first current pulse I_1 will change its state from 1 to 0. This generates a large induced voltage in the linking coil and drives Core 2 to state "1." After that the second current pulse I_2 shifts this state "1" back to Core 1 again. Thus the state "1" is transferred between Core 1 and Core 2 when the current pulses I_1 and I_2 are applied alternately. However, if both cores are originally in the "0" state, the I_1 pulse cannot change much of the flux of Core 1. The linking current is very small, and Core 2 remains in the "0" state. The alternate application of I_1 and I_2, which will be called advancing pulses from now on, therefore will not produce any change of the states of the cores. This constitutes a single-information storage, in which a binary digit can be stored indefinitely and read out at any given time by the application of a pair of advancing pulses.

Physically this is possible due to the existence of two limit cycles of the hysteresis loop when the two alternate advancing pulses are applied. As shown in Fig. 3, the upper loop represents the cyclic change of magnetization of cores when digit "1" is stored. The lower small loop represents the cyclic change of magnetization of cores when digit "0" is stored. In either case an advancing pulse changes the magnetization of one core along the curve a to b to c while that of the other core, through the linking coils, changes from c to d to a. Depending on the initial state of magnetization of the first core, the hysteresis loop follows either the upper or the lower curve.

III. PROPAGATION OF INFORMATION ALONG A DELAY LINE

The requirement for a magnetic delay line is that it should be able to store a series of information pulses and deliver them back at a later time. A number of magnetic cores are needed. These should be so constructed as to work in the following manner: When the first information pulse has been stored in the first magnetic core, an advancing pulse is applied to this core to transfer the information to the next core. This is necessary in order to make the first core ready to receive and store the second-information pulse. Next, these two signals are advanced further to make room for the storage of the third. This process of advancing and storing continues to the end of the line, where the information signal is sent out. If, after the line is loaded with information, no further advancing pulses are applied, the information will stay in the cores indefinitely. When advancing pulses are once again applied, the stored information is discharged. If the output of the delay line is connected to its input, a closed ring results. Information can be kept circulating around the ring continuously by the advancing pulses, and can be reproduced at any time. The same is true for magnetic recordings on a rotating storage drum, except that in the latter case the mechanical rotation of the drum is used to carry the information along, whereas in the present scheme advancing pulses are used to propagate the information.

Since all the magnetic cores in such a delay line are connected in tandem through the linking coils, two possible effects must be prevented before the desired information transfer can be made. First, an advancing pulse should advance a digit only in the forward direction; any backward flow of information is to be avoided. Second, an advancing pulse should advance a digit to the next core only; any effect of the digit on cores beyond this would interfere with previous digits. Of course it is imperative for successful operation that the signal should not fade along the line.

IV. A DELAY LINE OF THREE CORES PER BINARY DIGIT

A circuit has been developed which is based on the fundamental requirements of a delay line, discussed in Section III. The connections are shown in Fig. 4. Three cores are necessary for the storage of each binary digit. Three such cores together will therefore be referred to as one storage unit. Three successive pulses are required to advance the information from one storage unit to the next. These pulses, respectively, advance the signal from the first core to the second core,

[1] Chapter IV, Progress Report No. 2, November 10, 1948; the Computation Laboratory, Harvard University, under Contract W19-122-ac-24 with the U. S. Air Force.

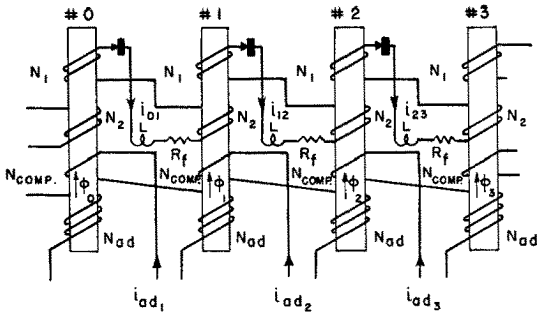

FIG. 4. Delay line structure of three cores per digit.

from the second core to the third core, and then from the third core to the first core of the next storage unit.

The operation can briefly be summarized as follows: All advancing pulses are connected so as to drive all the cores to negative saturation. When there is no information in the line, all the cores have negative residual magnetism and are thus in the "0" state. When information is stored, every third core may be positively or negatively magnetized and thus be in either state "1" or "0." Consider the case of a "0" being stored in Core 1. All advancing pulses are so connected so as to drive the cores to negative saturation. Since the residual magnetism on Core 1 is already negative and the core has essentially a square hysteresis loop, only a very small change of flux results when Advancing Pulse #1 is applied. There is no effect on other cores. The next core remains negatively magnetized. One can consider that the digit "0" information has been transferred to Core 2. On the other hand, if a "1" is stored in Core 1, it is positively magnetized. The application of i_{ad1} drives it to negative saturation. This large change of flux in Core 1 induces a large electromotive force in coils N_1 and N_2 of that core, causing i_{01} and i_{12} to flow. The current i_{12} drives Core 2 from negative magnetization to positive saturation.

The current i_{12} satisfies the following equation

$$N_1(d\phi_1/dt)+N_2(d\phi_2/dt)=[R_f+L(d/dt)]i_{12}, \quad (1)$$

where R_f represents the total resistance of the link circuit in the forward direction of i_{12} and L the leakage inductance of the linking coil. Integrating Eq. (1),

$$N_1\Delta\phi_1+N_2\Delta\phi_2=R_f\int i_{12}dt+L\Delta i_{12}.$$

Note that i_{12} is always a positive quantity due to the presence of the rectifier. Δi_{12} vanishes as the fluxes of Cores 1 and 2 reach a constant value. We get

$$\Delta\phi_2=-(N_1/N_2)\Delta\phi_1+R_f\int i_{12}dt. \quad (2)$$

The last term in Eq. 2 is always a positive quantity. If Cores 1 and 2 have the same dimensions, the flux change of ϕ_2 is not complete unless N_1 is greater than N_2. The optimum ratio of N_1 to N_2 is found to be close to 2:1.[2] The resultant change of flux of Core 2 has no effect on Core 3 because the linking current i_{23} is blocked by the rectifier in the circuit. This satisfies the requirement that information may not advance to cores beyond the next one. The current i_{01} is not desirable because it has the tendency to transfer information backward from Core 1 to Core 0. This current must be balanced by the use of a compensating winding, so that the net magnetizing force is always negative in Core 0 to maintain its negative saturation when information is being transferred from Core 1 to Core 2. Since this process of transfer affects only the three cores 0, 1, and 2, another digit in Core 4 can be transferred at the same time without interference in any other cores except 3, 4, and 5.

A static magnetic storage system is then obtained in which three cores are needed to store each binary digit. Information can be stored in the cores indefinitely and can be stepped along the line in the forward direction by the application of advancing pulses. Three advancing pulses are necessary to advance the information by a single storage unit.

Figure 5 shows a breadboard connection of such a delay line for the storage of four binary digits. The information can be advanced through each storage

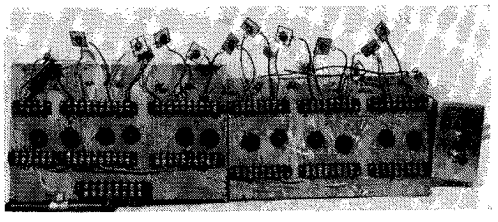

FIG. 5. Four binary digits delay line—three cores per digit.

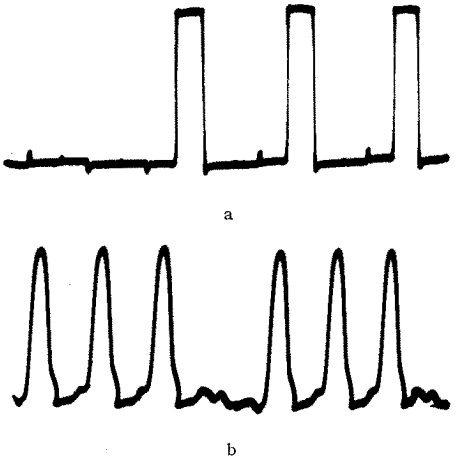

FIG. 6. Flux *vs.* time curve—three cores per digit. a. Information rate=3 kc. Information 0111. b. Information rate=30 kc. Information 1110.

[2] Chapter V, Progress Report No. 3, February 10, 1949; the Computation Laboratory, Harvard University, under Contract W19-122-ac-24 with the U. S. Air Force.

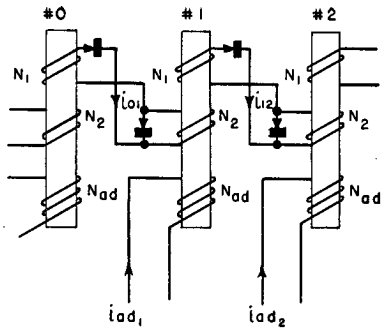

FIG. 7. Delay line structure of two cores per digit.

unit of three cores as fast as thirty thousand digits per second. Oscillographs showing flux variation of a core rate of 3000 and 30,000 digits per second are given in Fig. 6.

Small selenium rectifiers are used in the linking circuit. The rectifiers can be replaced by saturable reactors which offer a high reactance for current in one direction and a low reactance for current in the other direction. But since a reactor is not a highly dissipative element, its use prevents the linking current from dying down fast. This greatly reduces the maximum possible rate of advancing.

An analytical investigation of the sotrage unit in which rectifiers are used in the link circuits is given in reference 2.

V. A DELAY LINE OF TWO CORES PER BINARY DIGIT

As shown in the last section (Fig. 4), the compensating winding is necessary to counteract the effect of the current i_{01} flowing in the coil N_1 of Core 0. If this current can be eliminated, clearly no compensating winding is necessary. It can be done by the introduction of another rectifier,[3] as shown in Fig. 7. In the drawing the leakage inductance and circuit resistance have been omitted in the linking circuit for simplicity. The shunting of a rectifier across the coils N_2 is in such a direction that the current i_{12} is unaffected and produces the useful effect of transferring information from Core 1 to Core 2. But the current i_{01} is greatly reduced by the rectifier which short-circuits the electromotive force generated across N_2 of Core 1. The information then does not flow backward. Since only two cores are now involved in transferring the information, the next two cores can be used for another digit. It is then possible to use only two cores per binary digit.

Figure 8 shows an assembly of a delay line of this design to hold ten digits. Only two advancing pulses are needed to advance the information along the line. A few patterns of the flux variation in cores of this type of delay line are shown in Fig. 9, the repetition rate being 2.5 kc and 25 kc.

The only disadvantage of this connection is that the current flowing in coil N_2 of Core 1 is larger than before. This necessitates a more powerful advancing pulse to change the flux of Core 1.

Another possible arrangement is to apply a series voltage in the link 0–1 when i_{adv} is applied to Core 1 (Fig. 10). This series voltage is opposite to, and slightly greater than, the voltage generated in coil N_2 of Core 1. The transfer of information from Core 1 to Core 2 is made still easier. This scheme has also proved to be successful.

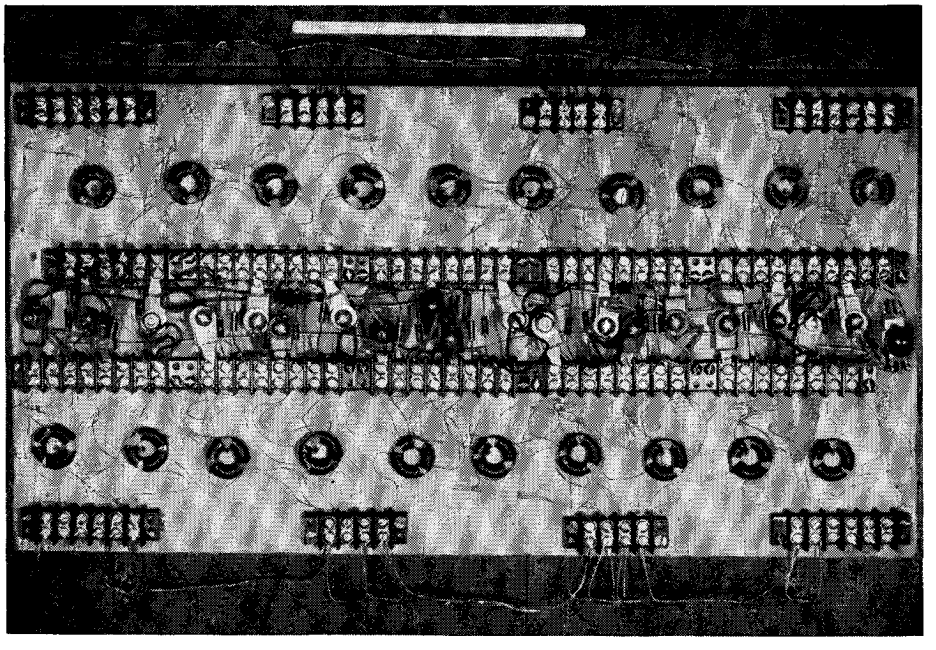

FIG. 8. Ten binary digits delay line—two cores per digit.

[3] Chapter V, Progress Report No. 4, May 10, 1949; the Computation Laboratory, Harvard University, under Contract W19-122-ac-24 with the U. S. Air Force.

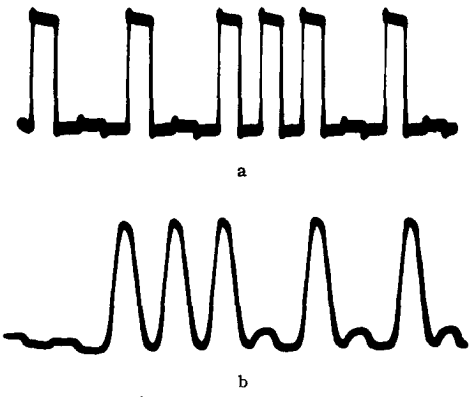

FIG. 9. Flux *vs.* time curve—two cores per digit. a. Information rate=2.5 kc. Information 1010111010. b. Information rate=25 kc. Information 0011101010.

VI. PROPERTIES OF MAGNETIC CORE MATERIAL

As shown in Fig. 11, the ideal hysteresis characteristics of the magnetic storage and delay line are a perfectly rectangular hysteresis loop and a very low coercive force.

In actual practice, unfortunately, such characteristics cannot be realized. Figure 12 shows a typical hysteresis curve for one of the cores manufactured by the Allegheny-Ludlum Steel Corporation of wound strips of Deltamax. The hysteresis loop is close to the ideal; nevertheless, the saturated region is not absolutely of zero slope, and the sharply rising portion is not quite vertical. In addition, the corners are somewhat rounded. But delay lines using such cores have been constructed and operate reliably. The criteria of how good the hysteresis loop is must have been discussed in reference 2.

As the frequency of operation becomes higher, the hysteresis and eddy current losses become appreciable. The heat generated is considerable at the highest frequency of operation. Moreover, the eddy current acts like a short-circuited secondary around the core. The presence of the eddy current requires a larger advancing current to drive the core from one polarity to the other.

At an operating frequency of 50 kc, every core alternates its flux between two saturation values in 10 microseconds. Assume that the flux changes linearly. This is a fairly accurate assumption, as seen from an oscillograph of flux variation. The cores used are made of a strip of one-mil thickness, $\frac{1}{8}$ inch wide, wound into a single-turn core of $\frac{1}{2}$-inch diameter. The hysteresis loss is estimated to be of the order of 7 milliwatt/core, the eddy current loss 25 milliwatt/core, the electrical resistivity of the core being taken as 50 microhm centimeters. For such a core the equivalent demagnetizing ampereturns can be calculated to be about 1.2. It is also equivalent to an increase of coercive force of 0.37 oersted. Apart from the upper frequency limits imposed by these losses, the fundamental operation of the storage and delay line is independent of the frequency.

VII. APPLICATIONS

It may be helpful to point out the unique features of this form of storage. No power is needed to maintain the storage of information. No mechanical movement is needed in recording and pick-up. The speed of recording, transfer, and read out has no lower limit and can be varied to an upper limit which is sufficiently high to be very useful. At the present stage, this maximum rate is of the order of 50 kc. These features represent improvements over the characteristics of the storage devices mentioned in the introduction.

Possible applications include the following:

1. *Information storage.* Individual binary digits can be stored in pairs of cores, as discussed in Section II. If a series of digits is to be stored, the information can be sent into a delay line. After the whole series of digits is in the line, stopping the flow of advancing pulses suffices to store the information indefinitely in the line. It can be read out at any time at the end of the line by applying the advancing pulses again. Development work is being done at the Computation Laboratory of Harvard University to construct a line holding 40 binary digits in a plug-in component container unit which will be no more than two inches in diameter and six inches in length.

2. *Input and output link for high speed computers.* This form of delay line provides an excellent medium for transfer of information between systems of different digital rate. Data and commands can be put into the line manually and then read out to the machine at its operating speed. Again, results from the machine can be fed at high speed into the delay line, from which later a set of slow advancing pulses can step the results out at a speed suitable, say, to operate a typewriter directly.

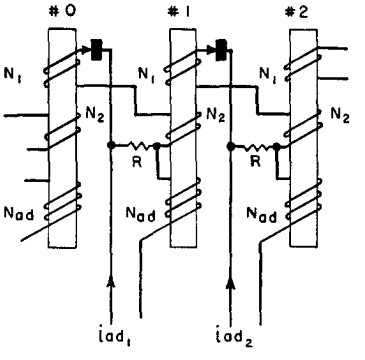

FIG. 10. Another form of delay line of two cores per digit.

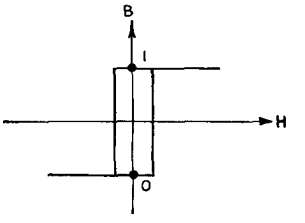

FIG. 11. Ideal hysteresis loop.

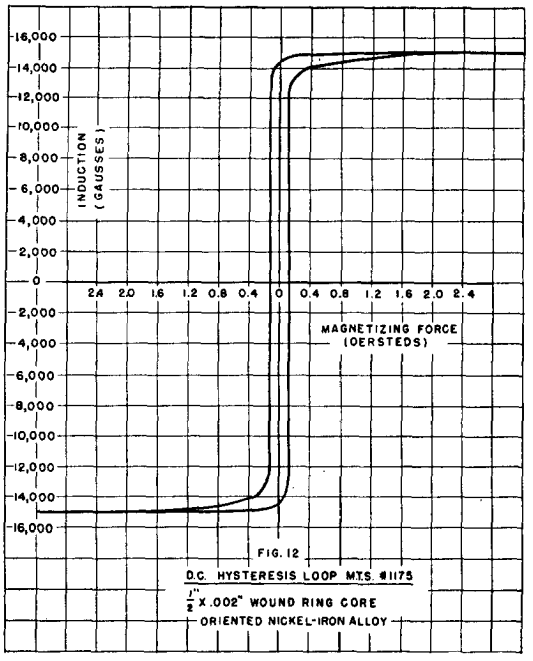

FIG. 12. Typical hysteresis loop of materials used.

3. *Counter.* Since the information stored in the delay line must be stepped along by advancing pulses, it is possible to register a single digit at the beginning of the line, and by the location of this digit along the line at a later instant to determine the number of advancing pulses that have been applied. So far the speed of counting is limited to about 50 kc. This, however, is sufficiently rapid to find wide applications.

4. *Telegraphy.* Because the speed of propagation is variable, a magnetic delay line may serve as the terminal storage for a high speed telegraphy system. The information on a high speed telegraphic line can be distributed to several delay lines. While some lines are being filled, any one of them can be discharged much more slowly to a separate line or directly to a typewriter. Similarly, several slow speed information sources can be read into the magnetic delay lines and then be fed into a high speed telegraphic line by electronic switching control of the advancing pulses.

VIII. ACKNOWLEDGMENTS

The magnetic core materials employed in this research were supplied by the Allegheny Ludlum Steel Corporation, whose cooperation and assistance the authors wish to acknowledge. The use of magnetic cores as a means of obtaining static magnetic storage was originally proposed by Howard H. Aiken, director of the Computation Laboratory, who has worked closely with the authors.